



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,500	07/26/2001	Haeng-Seon Kim	06192.0197.NPUS00	6260

7590 02/27/2003
McGuire Woods LLP
1750 Tysons Boulevard
Suite 1800
McLean, VA 22102

EXAMINER

LESPERANCE, JEAN E

ART UNIT PAPER NUMBER

2674

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/912,500

Applicant(s)

KIM, HAENG-SEON

Examiner

Jean E Lesperance

Art Unit

2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 July 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claims 1-10 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 are rejected under 35 U.S.C. 102 (e) as being unpatentable over U.S. Patent # 6,229,513 ("Nakano et al.").

As for claims 1 and 6, Nakano et al. teach a display timing signal DTMG are sent from the computer side in accordance with a LVDS scheme (column 4, lines 54-58) corresponding to a system including an image processing part for deciding a timing format of an image data and generating a control signal for the image data, the voltage level of display data must be converted to a high voltage range... column 10, lines 61-64) corresponding to an encoder for encoding the image data and the display control unit 110 outputs an output polarity control signal to the drain drivers 130 through the signal line 135 (column 6, lines 46-49) corresponding to the control signal output from the image processing part in an RSDS specification, power supply circuit (120)

Art Unit: 2674

corresponding to a power output part for outputting a constant-voltage; and an interface unit Fig.1 (100) corresponding to a control board including a power supply part for converting the constant-voltage of the power output part into a predetermined voltage level, positive voltage generator (121) corresponding to a gray scale generating part for generating a gray scale voltage using the predetermined voltage level of the voltage converting part, gate electrode drive voltage generator (124) corresponding to a gate voltage generating part for generating a gate on/off voltage using the predetermined voltage level of the voltage converting part, and transmission line (134) corresponding to a transmission line for transmitting the encoded image data and the control signal; the gate drivers Fig.1 (140) corresponding to a first connecting member having a data driver for generating a column signal when the image data, the control signal and the gray scale voltage are applied; the drain drivers Fig.1 (130) corresponding to a second connecting member having a scan driver for generating a scan signal when the control signal and the gate on/off voltage are applied; and liquid display panel Fig.1 (10) corresponding to a flat panel for forming a picture using the scan signal and the column signal.

As for claims 2 and 7, Nakano et al. teach a low voltage decoder (ig.8 (279) corresponding to a first decoding means for decoding the data and the control signal of the data; a shift register Fig.7 (153) corresponding to a first register means for temporarily storing the data decoded by the first decoding means; and a shift register 153 in a control circuit 152 of the drain driver 130 generates a data fetch signal for an input register 154 based on a clock D4 or D5 for latching display data inputted from the

display control unit 110, and outputs the data fetch signal to the input register 154 (column 9, lines 61-65) corresponding to a first signal processing means for generating and outputting a column signal using the data stored in the first register means, the control signal and the gray scale voltage.

As for claims 3 and 8, Nakano et al. teach the $2n$ originally ordered display data transmitted..... (column 7, lines 9-17) and the clock signals D4, D5, which is the same frequency as that of the display data, are transmitted alternately to the groups A and B of the drain drivers 130.... (column 7, lines 33-42) corresponding to the data and the control signal are transmitted in a mixed signal within a single channel, are decoded by the first decoding means, are divided to be stored at a first register and a second register of the first register means, and are output to the first signal processing means.

As for claim 4 and 9, Nakano et al. teach (Fig.7) with a data bus 134 which is separately transmitted from the clock signal D1 and alternating signal M from signal line 135 corresponding to the data and the control signal are separately transmitted through respective corresponding channels, the level shifters 156 convert the voltage levels of display data to higher levels and the high voltage signal decoders 278 and low voltage signal decoders 279 are both formed of high break-down MOS transistors (column 11, lines 4-8) corresponding to are respectively decoded by a first decoder and a second decoder of the first decoding means, the storage register B (155) and the level shifter (156) corresponding to are divided to be stored at a third register and a fourth register of the first register means, and are output to the first signal processing means.

As for claims 5 and 10, Nakano et al. teach the high voltage and low voltage decoders Fig.8 (261) corresponding to a second decoding means for decoding the control signal; the input registry B Fig.7 (154) corresponding to a second register means for temporarily storing the control signal decoded by the second decoding means; and the display control unit outputs a frame start instruction signal to the gate drivers 140 through a signal line 142, and outputs a shift clock signal G1 to sequentially selecting each gate signal line G of the liquid crystal panel 10 to gate drivers 140 through a signal line 141 for every one horizontal scan period (column 6, lines 50-56) corresponding to a second signal processing means for generating a scan signal using the control signal stored in the second register means and the gate on/off voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:00AM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

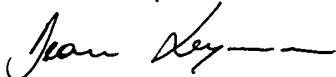
Art Unit: 2674

(703) 872-9314 (for Technology Center 2600 only)

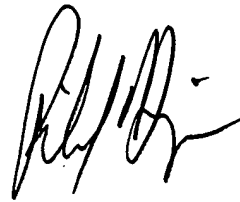
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance


Art Unit 2674

Date 2-20-2003



RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600